



# UNITED STATES PATENT AND TRADEMARK OFFICE

*W*

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/662,459	09/16/2003	Steven N. Bathiche	003797.00546	9612

28319 7590 08/16/2006

BANNER & WITCOFF LTD.,  
ATTORNEYS FOR CLIENT NOS. 003797 & 013797  
1001 G STREET, N.W.  
SUITE 1100  
WASHINGTON, DC 20001-4597

EXAMINER
----------

PHAM, TAMMY T

ART UNIT	PAPER NUMBER
----------	--------------

2629

DATE MAILED: 08/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	10/662,459	BATHICHE, STEVEN N.	
	Examiner	Art Unit	
	Tammy Pham	2629	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 23 May 2006.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 2,4-21 and 23-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 2,4-21 and 23-25 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>7-24-06</u>   | 6) <input type="checkbox"/> Other: _____                                    |

**DETAILED ACTION**

***Response to Amendment***

Claims 1, 3, 22 have been cancelled. Claims 2, 4, 7, 8, 11, 17, 18 and 21 have been amended.

Claims 23-25 have been added. Claims 2, 4-21, 23-25 are pending.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 2, 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barker et al. (US Patent No: 5,675,329).

**As for claims 4, 7, Barker teaches of a computer keyboard (11), comprising:**

a plurality of keys (11), each key (11) of the plurality having an unpressed condition in which no force is exerted upon the key (11) by a user (Fig. 2, first period as described in step 110) and a pressed condition in which force is exerted on the key (11) by a user (Fig. 2, second period as described in step 140) in column 2, lines 34-41; and

a force detection circuit (12) configured to:

scan each key (12) of the plurality to determine if a scanned key (12) is in a pressed condition (see Fig. 2, step 110),

quantify, upon determining that a scanned key (11) is in a pressed condition, the force exerted by a user on the key (11) determined to be in a pressed condition (Fig. 2, step 120), and

proceed, upon determining that a scanned key (11) is not in a pressed condition, to another key (11) of the plurality without attempting to determine a force exerted on the key (11) determined not to be in a pressed condition in column 4, lines 12-23 and in Fig. 2, step 180 (if the user did not exert force upon the key, the force would not attempt to quantify the force exert upon the key but instead the apparatus awaits until a key qualifies under one of the two conditions for step 180 as depicted in Fig. 2).

In column 2, line 57 and 59; he mentions that his apparatus is able to incorporate capacitive technologies and a force sensing resistor; since the definition of an RC network is basically a circuit that encompasses at least one resistor and one capacitor; Barker teaches that the detection circuit includes an RC network {claim 7}.

Barker fails to explicitly teach of first and second conductors in which the force sensitive resistive elements resides in between and of a voltage divider that is a part of the force detection circuit.

However, in column 2, lines 53-55, Barker teaches that the force sensing device can detect the pressure of force exerted on any of the key on the keyboard. It is known in the art to include a first group of conductors;

a second group of conductors positioned in close proximity to the first group of conductors, the first and second groups of conductors forming a plurality of intersections between first group conductors and second group conductors; and

a force sensitive resistive element (12) located between the first group conductor and the second group conductor of each of the plurality of intersections,

each of the plurality of intersections corresponds to an associated key (11) of the plurality of keys (11), each of the associated keys (11) configured to compress the resistive element located at the corresponding intersection upon exertion of force on the associated key (11), and

the force detection circuit (12) is configured to determine force exerted upon each of the associated keys (11) based upon changes in resistance value of the resistive element at each corresponding intersection.

It would have been obvious to one with ordinary skill in the art at the time the invention was made to combine have the force detection circuit be between two conductive layers which corresponds to an associated key with the force detection circuit of Barker in order to detect the force exerted upon each of the keys on the keyboard.

Barker goes on to teach of the force detection circuit (12) comprises a microprocessor (18) and of a first condition when scanning each key (11) of the plurality to determine if a scanned key is in a pressed condition (see Fig. 2, first period of step 110) and in a second condition when quantifying the force exerted by a user on a key (11) determined to be in a pressed condition (see Fig. 2, second period of step 140) in column 3, line 50.

It is well known in the art to include a voltage divider with a force detection circuit.

It would have been obvious to one with ordinary skills in the art at the time the invention was made to include with the force detection circuit as taught of Barker a voltage to provide an easy and well known method to control the voltage going through the circuit.

**As for claim 2**, Barker teaches of the plurality of keys includes multiple character keys having respective characters assigned thereto and a plurality of modifier keys, and wherein the force detection circuit (12) comprises a microprocessor (18) configured to generate a first signal upon detecting a character key to be in a pressed condition and to generate a different signal upon detecting the character key and a modifier key to simultaneously be in a pressed condition in column 1, lines 28-44.

**As for claim 5**, Barker teaches and of the voltage divider (well known as discussed above) includes a voltage measuring node (inherent),

force detection circuit (12) is in the first condition (Fig. 2, first period of step 110), voltage at the voltage measuring node varies within a first range (Fig. 2, normal force) as a key is pressed,

when the force detection circuit (12) is in the second condition (see Fig. 2, second period of step 140), voltage at the voltage measuring node varies within a second range (Fig. 2, second activating force) as a key is pressed, and

the second range is larger than the first range in column 4, lines 10-25.

**As for claim 6**, Barker teaches of an Analog to Digital Converter (16), and wherein:

the microprocessor (18) determines a scanned key is in a pressed condition when voltage on a tested conductor of the corresponding intersection reaches a threshold value, and

Art Unit: 2629

the microprocessor (18), after determining the scanned key is in a pressed condition, instructs the ADC (16) to output a digital value of a voltage on the tested conductor in column 2, lines 65-67.

2. Claims 8-21, 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barker et al. (US Patent No: 5,675,329) in view of Olodort et al. (US Patent No: 6,563,434 B1).

**As for claim 8**, Barker teaches of a computer keyboard (11), comprising a plurality of keys (11) located above the plurality of intersections, each key (11) being associated with one intersection and configured to exert force on the conductors and force-sensitive resistive element of the associated intersection during a key press (11) in column 2, line 54;

a microprocessor (18);

and an Analog to Digital Converter (16) coupled to the microprocessor (18)

Barker fails to teach of a first and second group of conductors which the force sensitive resistive element is located in between and of a sub-circuit to at least one of the second group conductors, the sub-circuit having a resistor network switchable by the microprocessor (18) between a low resistance value and a high resistance value;

However, in column 2, lines 53-55, Barker teaches that the force sensing device can detect the pressure of force exerted on any of the key on the keyboard. It is known in the art to include a grid of first group conductors and a second group conductors, the first and second

Art Unit: 2629

group conductors forming a plurality of intersections; a force-sensitive resistive element at each intersection of the plurality located between one of the conductors of the first group and one of the conductors of the second group forming the intersection;

It would have been obvious to one with ordinary skill in the art at the time the invention was made to combine have the force detection circuit be between two conductive layers which corresponds to an associated key with the force detection circuit of Barker in order to detect the force exerted upon each of the keys on the keyboard.

Olodort teaches of a sub-circuit (Fig. 40) connected to conductors (inherent), the sub-circuit (Fig. 40) having a resistor network switchable by the microprocessor (650) between a low resistance value (column 19, line 8) and a high resistance value (column 19, line 5).

It would have been obvious to one with ordinary skill in the art at the time the invention was made to combine the sub-circuit of Olodort with the force detection circuit of Barker in order to a more space efficient way to detect key actuation in a keyboard assembly (see column 2, line 33).

**As for claim 9**, Olodort teaches of the microprocessor (650).

ground to an individual conductor pin (column 19, line 8),

test another conductor pin for a threshold voltage level while the resistor network (Fig. 41) is switched to the high resistance value (binary value 1, aka, while the bus is grounded and hence in a high resistive state, the circuit is able to detect if any of the keys are pressed, column 19, line 9),



switch the resistor network to the low resistance (binary value 2) value upon detecting the threshold voltage level on the tested conductor pin in column 19, lines 13-20, and

receive from the ADC (611) a digital value of a voltage on the tested conductor pin while the resistor network is switched to the low resistance (binary value 1) value in column 19, lines 13-20.

As for **claim 10**, Olodort teaches of a plurality of sub-circuits (Fig. 40) connected to a plurality of conductors of the second group of conductors (the conductors connected to bus when the circuit is in a binary 2 state) in column 19, line 18.

As for **claims 11, 19**, Barker teaches of the microprocessor (18) is configured to: store the identity of a plurality pressed keys (11) and force values associated with the pressed keys (11), and generate a data message containing the identities and associated force values in column 3, line 2. The passage shows that the microprocessor is able to identify the key and the force and communicate this data to the rest of the apparatus accordingly so that the desired output is conducted.

As for **claims 12, 20**, Barker teaches of the microprocessor (18) is configured to generate the data message in column 4, lines 25-40.

Barker does not teach that the data message is in the form of a Human Interface Device (HID) report.

Art Unit: 2629

Applicant has not disclosed any specific advantage or criticality to using the HID. As such, the data message in the form of HID is an obvious matter of design choice.

Therefore, it would have been obvious to generate the data message in the form of HID, since any form would perform equally well at transmitting data to and from the microprocessor.

**As for claim 13**, Barker teaches that the plurality of keys (11) includes multiple character keys having respective characters assigned thereto and a plurality of modifier keys in column 4, lines 25-40.

**As for claims 14, 21**, Barker teaches of the plurality of keys (11) includes at least 36 character keys {claim 14} and of scanning the keyboard (11) for presses of additional keys (11) comprises testing for a threshold voltage level with regard to at least 35 separate keys (11) {claim 21} in column 2, line 52.

**As for claim 15**, Olodort teaches that microprocessor (18) is configured to sequentially test each key for a key (740) press by grounding a conductor pin connected to one of the conductors forming the associated intersection (column 19, line 8) and testing for the threshold voltage level on the other of the conductors forming the associated intersection (column 19, line 8), and receive, for only the keys (740) for which the threshold voltage level was detected, the digital value from the ADC (611) in column 18, line 45.

As for claim 16, Barker teaches of the microprocessor (18) is configured to generate a data message (key scan data byte) containing identifiers for multiple keys (11) of the plurality for which the threshold voltage level was detected and digital values from the ADC (16) corresponding to the multiple keys (11) in column 2, line 9.

As for claim 17, Barker teaches of a microprocessor (18) having preprogrammed instructions for performing steps comprising a detection circuit (12).

Barker fails to teach of the various states of the detection circuit.

Olodort teaches of a first state (binary level 1) in which the detection circuit (Fig. 41) is configured to identify a pressed key of a keyboard (740) in column 19, line 9;

selecting, while in the first state (binary level 1), a conductor pin from a group of conductor pins;

testing, while in the first state (binary level 1), the selected conductor pin for a threshold voltage level in column 19, line 15;

upon detecting the threshold voltage level on the selected conductor pin, placing the detection circuit (Fig. 41) in a second state (binary level 2) by altering the resistance of a resistance network (Fig. 41) in column 19, line 22;

when in the second state (binary level 2), receiving a digital value (612) for a voltage on the selected conductor pin, the digital voltage value (612) representing an amount of force applied to the pressed key (the signal represents the key pressed, see column 18, lines 45-48);

scanning the keyboard (600) for presses of additional keys by testing for a threshold voltage level with regard to each key (600) for a key press when the detection circuit (Fig. 41) is in the first state (binary level 1) in column 19, line 8; and

measuring the detection circuit (Fig. 41) in the second state (binary level 2) and receiving additional digital voltage (612) values upon of threshold voltages with regard to the additional keys (600) in column 19, line 16.

It would have been obvious to one with ordinary skill in the art at the time the invention was made to combine the sub-circuit of Olodort with the force detection circuit of Barker in order to a more space efficient way to detect key actuation in a keyboard assembly (see column 2, line 33).

**As for claim 18**, Barker teaches of having additional preprogrammed instructions for performing steps comprising instructing an Analog to Digital Converter (16) to convert a detection circuit voltage (12) to a digital value and reading from the ADC (16) a digital value for the detection circuit voltage (12) in column 2, line 67.

**As for claim 23**, Olodort teaches of placing the voltage divider (614, 618) in the second condition (binary level 2) comprises altering a resistance value in a portion of the voltage divider (614, 618), the altered resistance value portion not including one of the force sensitive resistive elements in column 19, line 8 and line 19.

**As for claim 24**, neither Barker nor Olodort have any mention of using a time constant from an RC network in order to configurate the force exerted on the keyboard.

Exminer takes official notice that it is well known in the art to have microprocessor configured to determined force exerted on one of the associated keys based on a time constant for the RC network.

It would have been obvious to one with ordinary skill in the art at the time the invention was made to combine use the time constant from an RC network in order to determine the force exerted on the keyboard because it provides an easy method that utilizes the existing information from an RC network to determine the force applied.

**As for claim 25**, Olodort teaches placing the detection circuit (Fig. 41) in a second state (binary state 2) by altering the resistance of a resistance network (Fig. 41) comprises altering a resistance value in a portion of the resistance network (Fig. 41) that does not include a force sensitive resistive element in column 19, line 8 and line 19.

### ***Response to Arguments***


Applicant's arguments with respect to claims 2, 4-21, 23-25 have been considered but are moot in view of the new ground(s) of rejection.


***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tammy Pham whose telephone number is (571) 272-7773. The examiner can normally be reached on 8:00-5:30 (Mon-Fri).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

  
Tammy Pham  
August 13, 2006

  
RICHARD HJERPE  
SUPERVISORY PATENT EXAMINER  
TECHNICAL CENTER 2600